



Job Profile

Senior ASIC Engineer

Scope

To efficiently implement and verify on-chip DSP filtering and control-loop algorithms.

Key Accountability Areas

1. Design digital blocks that are area-efficient, low-power, maintainable and on schedule.
2. Lead the development of structured verification strategies at both chip and block levels.
3. Develop strong methodologies for design that can be used by the entire team.

Typical Activities

- RTL development and verification in Verilog.
- Develop automated design verification test suites.
- Develop C-based unit tests for blocks.
- Develop PERL or TCL scripts as required to aid in design verification.
- RTL lint checking, and code coverage.
- Area and power optimization.
- Reviewing synthesis timing reports, and optimizing associated critical timing paths.
- Prepare design documentation, test plans and reports.
- Provide technical mentoring to junior engineers.
- Meet with project leads from other teams to establish project work plans.

Requirements

- Extensive experience in digital design using Verilog.
- Experience with Cadence toolset is preferred (RTL compiler, NC-Sim).
- Proficient programming in PERL, TCL and C.
- Knowledge of Matlab or Octave is a plus.
- Knowledge of digital communications, DSP, analog and digital video standards is an asset.
- Proven track record in first-time right designs.
- Hands-on lab experience testing silicon.
- Innovative and clear thinker.
- Strong communication skills.
- Self motivated.
- Effective team collaborator.
- Leadership qualities.
- 8+ years of R&D experience in a related industry, minimum 5 years in ASIC design.
- Bachelor degree in Electrical Engineering.