



Job Description

Senior ASIC Engineer

Scope

To efficiently implement and verify DSP filtering and control-loop algorithms in hardware, with a focus on achieving "first-time right" silicon.

Key Accountability Areas

- Design digital blocks that are area-efficient, low-power, maintainable and delivered on schedule.
- Provide leadership to the ASIC design team to ensure correct design decisions are made at each stage of the development process.

Typical Activities

- RTL development and verification in Verilog.
- Development automated design verification test suites.
- Development of C-based unit tests for blocks.
- Develop PERL or TCL scripts as required to aid in design verification.
- RTL lint checking, and code coverage.
- Area and power optimization.
- Reviewing synthesis timing reports, and optimizing associated critical timing paths.
- Prepare design documentation, test plans and reports.
- Provide technical mentoring to junior engineers.
- Meet with project leads from other teams to establish project work plans.

Requirements

- Extensive experience in digital design using Verilog.
- Experience with Cadence toolset is preferred (RTL compiler, NC-Sim).
- Proficient programming in PERL, TCL and C.
- Knowledge of Matlab or Octave is a plus.
- Knowledge of digital communications, DSP, and analog/digital video standards is an asset.
- Hands-on lab experience testing silicon.
- Proven track record in first-time right designs.
- Innovative and clear thinker.
- Strong communication skills.
- Self motivated.
- Effective team collaborator.
- Leadership qualities.
- 8+ years of R&D experience in a related industry, minimum 5 years in ASIC design.
- Bachelor degree in Electrical Engineering.